1. One data type and one timing (control) type input. (2 inputs)
2. For a D latch, as long as the timing input is asserted, the output will match the input D. When the control is un-asserted the output will memorize the last held value of D.  
   For a D flip-flop, the output will update its state to D’s as the clock/control asserts. No matter what d does while the control is asserted or de-asserted, the output will remain the same until the instant the clock asserts again. That is unless the reset is asserted.

